

U.S. DEPARTMENT OF COMMERCE  
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**UTILITY PATENT APPLICATION  
TRANSMITTAL LETTER  
UNDER 37 C.F.R. 1.53(b)**

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Address to:  
Assistant Commissioner for Patents  
Washington D.C. 20231  
Box Patent Application

Transmitted herewith for filing is the patent application of

Inventor(s): **Martin VORBACH and Robert MÜNCH**

For : I/O AND MEMORY BUS SYSTEM FOR DFPS AND UNITS WITH TWO-  
OR MULTI-DIMENSIONAL PROGRAMMABLE CELL  
ARCHITECTURES

Enclosed are:

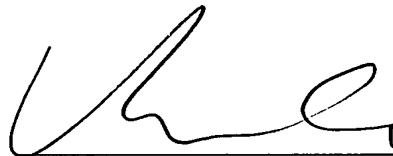
1. 31 sheets of specification, 3 sheets of claims, and 1 sheet of abstract.
2. 18 sheets of drawings.
3. Also enclosed:  
Return Receipt Postcard.
4. Related Application:

This application is a continuation of International Patent Application  
PCT/DE97/03013 filed on December 21, 1997 and a continuation-in-part of U.S.  
Patent Application Ser. No. 08/947,254 filed on October 8, 1997.

5. The filing fee is not being paid at this time.

Dated: *18 June 1999*

By:



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**DATE OF DEPOSIT** 6/18/99

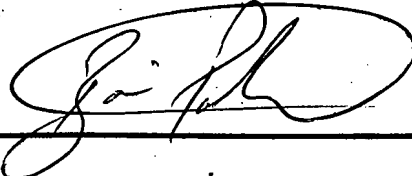
**TYPE OF DOCUMENT** PATENT APPLICATION OF VORBACH ET AL

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TITLE: I/O AND MEMORY BUS SYSTEM FOR DFPS AND UNITS WITH  
TWO OR MULTI-DIMENSIONAL PROGRAMMABLE CELL ARCHITECTURES